DH251 Hall-effect sensor is a temperature stable, stress-resistant, Low Tolerance of Sensitivity micro-power switch. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

DH251 is special made for low operation voltage, 1.65V, to active the chip which is includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, CMOS output driver. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, very low input-offset errors, and small component geometries. This device requires the presence of omni-polar magnetic fields for operation.

The package type is in a Halogen Free version has been verified by third party Lab.

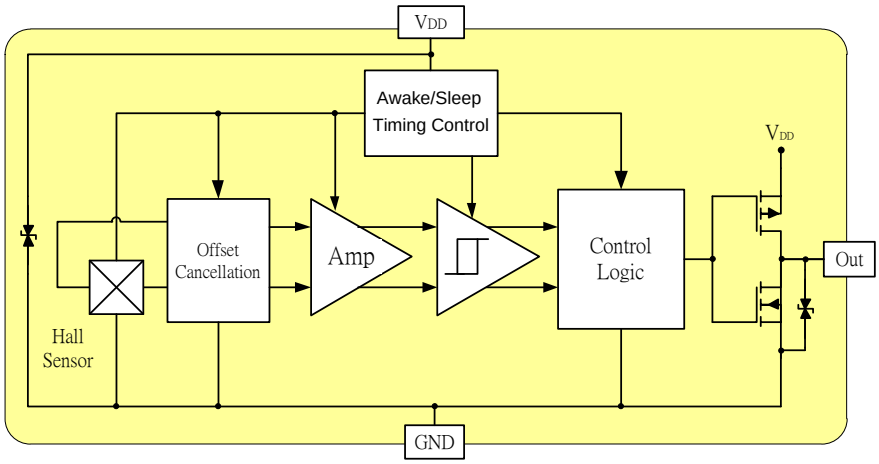
Features and Benefits

- CMOS Hall IC Technology
- Strong RF noise protection
- 1.65 to 6 V for battery-powered applications
- Omni polar, output switches with absolute value of North or South pole from magnet
- Operation down to 1.65V, Micro power consumption
- High Sensitivity for reed switch replacement applications
- Multi Small Size option
- Low sensitivity drift in crossing of Temp. range
- Ultra Low power consumption at 5uA (Avg)
- High ESD Protection, HMB > ±4KV(min)
- Totem-pole output

Applications

- Solid state switch
- Handheld Wireless Handset Awake Switch (Flip Cell/PHS Phone/Note Book/Flip Video Set)
- Lid close sensor for battery powered devices
- Magnet proximity sensor for reed switch replacement in low duty cycle applications
- Water Meter
- Floating Meter
- PDVD
- NB

Functional Diagram



***Note**: Static sensitive device; please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100 Ω resistor in series with V_{DD} is recommended.*
D H 25 1, HBM > ±4KV which is verified by third party lab.

Absolute Maximum Ratings *At(Ta=25 ℃)*

Characteristics		Values	Unit
Supply voltage,(V_{DD})		7	V
Output Voltage,(V_{out})		7	V
Reverse Voltage , (V_{DD}) (V_{OUT})		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current,(I_{OUT})		1	mA
Operating temperature range, (Ta)		-40 to +85	℃
Storage temperature range, (Ts)		-65 to +150	℃
Maximum Junction Temp,(Tj)		150	℃
Thermal Resistance	(θ_{JA}) ST / SN / UA / SQ	310 / 540 / 206 / 543	℃/W
	(θ_{JC}) ST / SN / UA / SQ	223 / 390 / 148 / 410	℃/W
Package Power Dissipation, (P_D)	ST / SN / UA / SQ	400 / 230 / 606 / 230	mW

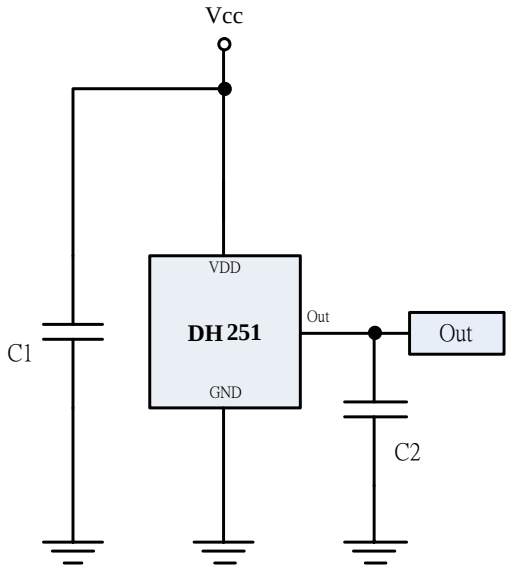
***Note:** Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.*

Electrical Specifications

DC Operating Parameters：Ta=25℃, V_{DD}=1.8V

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage,(V_{DD})	Operating	1.65		6	V
Supply Current,(I_{DD})	Awake State		1.4	3	mA
	Sleep State		3.6	7	μA
	Average		5	10	μA
Output Leakage Current,(I_{off})	Output off			1	uA
Output High Voltage,(V_{OH})	I_{OUT}=0.5mA(Source)	V_{DD}-0.2			V
Output Low Voltage,(V_{OL})	I_{OUT}=0.5mA(Sink)			0.2	V
Awake mode time,(T_{aw})	Operating		40	80	uS
Sleep mode time,(T_{SL})	Operating		40	80	mS
Duty Cycle,(D,C)			0.1		%
Electro-Static Discharge	HBM	4			KV
Operate Point, (B_{OPS})	S pole to branded side, B > BOP, Vout On		30	55	Gauss
(B_{OPN})	N pole to branded side, B > BOP, Vout On	-55	-30		
Release Point (B_{RPS})	S pole to branded side, B < BRP, Vout Off	10	20		Gauss
(B_{RPN})	N pole to branded side, B < BRP, Vout Off		-20	-10	
Hysteresis,(B_{HYS})	|BOPx - BRPx|		10		Gauss

Typical Application circuit



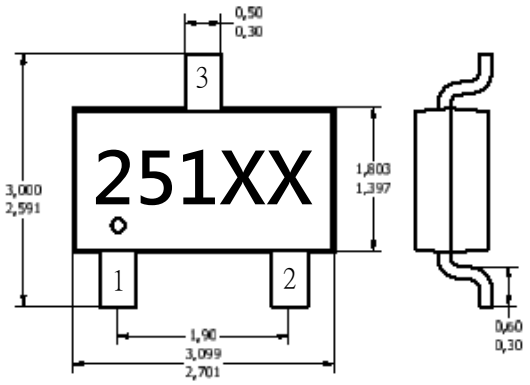
C1：10nF
C2：100pF

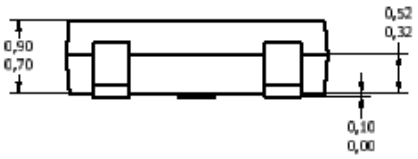
Sensor Location, package dimension and marking

DH251 Package

ST Package(TSOT-23)

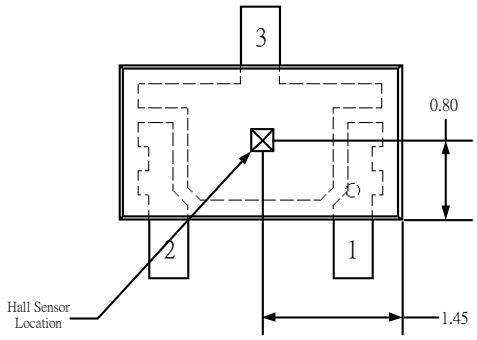
(Top View)





Hall Plate Chip Location

(Bottom view)



NOTES:

1. PINOUT (See Top View at left:)

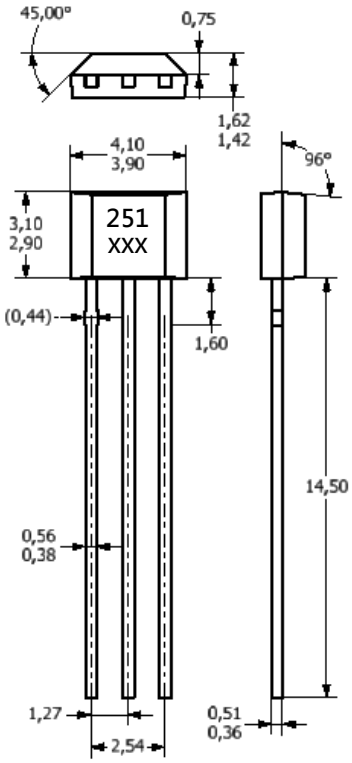
   Pin 1 VDD

   Pin 2 Output

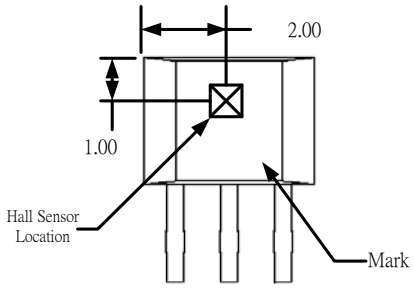
   Pin 3 GND

2. Controlling dimension: mm;

UA Package



Hall Chip location



NOTES:

1).Controlling dimension: mm 2).Leads must be free of flash and plating voids

3).Do not bend leads within 1 mm of lead to package interface.

4).PINOUT:

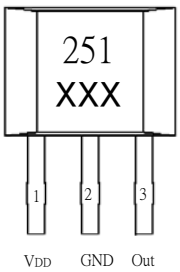
Pin 1 VDD

Pin 2 GND

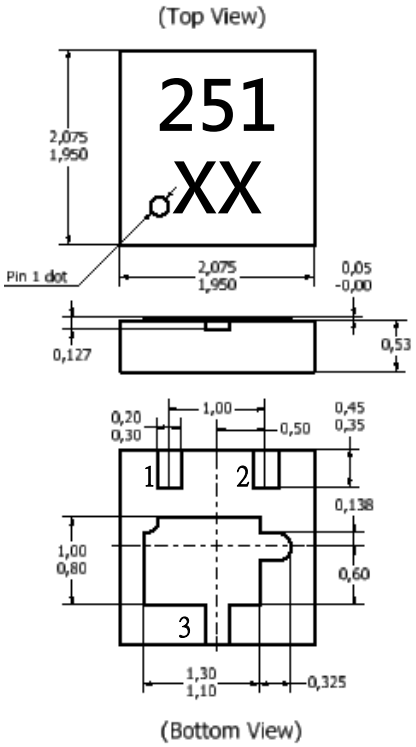
Pin 3 Output

Output Pin Assignment

(Top view)



SQ Package



NOTES:

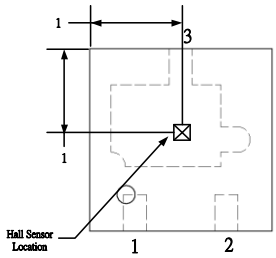
3. PINOUT (See Top View at left)

   Pin 1 VDD

   Pin 2 Output

   Pin 3 GND

4. Controlling dimension: mm;

5. Chip rubbing will be 10mil maximum;

6. Chip must be in PKG. center.